January 1990
Revised December 1998

74ACT899
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The ACT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. The ACT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

Features

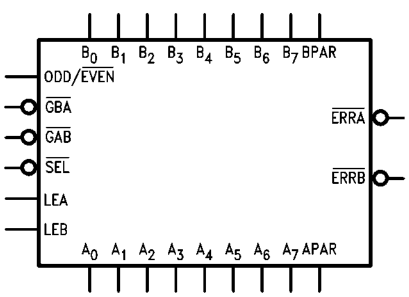
- Latchable transceiver with output sink of 24 mA
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enable for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in system applications in place of the 280
- May be used in system applications in place of the 657 and 373 (no need to change T/$\overline{\text{R}}$ to check parity)

Ordering Code:

Order Number	Package Number	Package Description
74ACT899QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450" Square

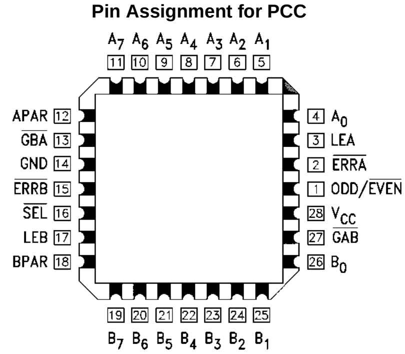
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram

Pin Assignment for PCC



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Pin Descriptions

Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The ACT899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table).

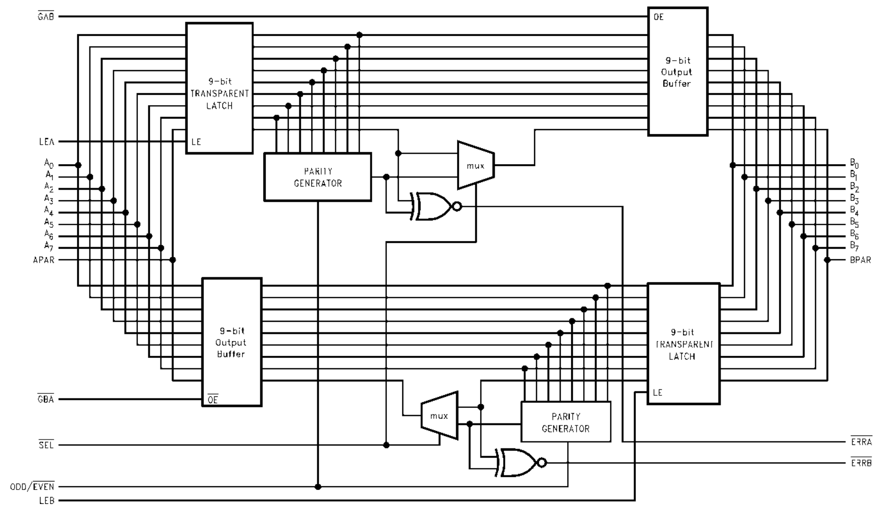
Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are 3-STATE.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

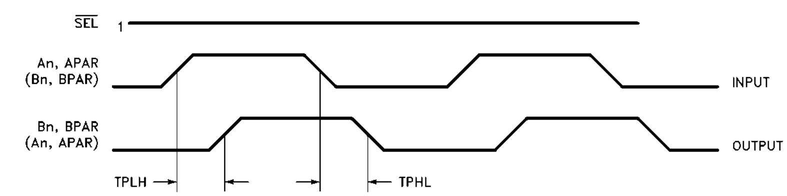
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: O/$\overline{\text{E}}$ = ODD/$\overline{\text{EVEN}}$

Functional Block Diagram



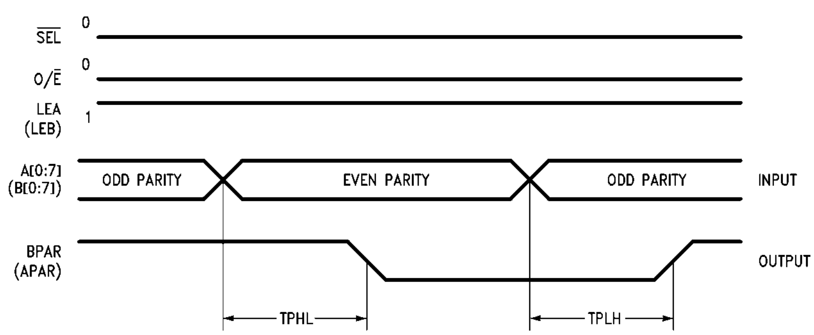
AC Path



A_n, APAR → B_n, BPAR

(B_n, BPAR → A_n, APAR)

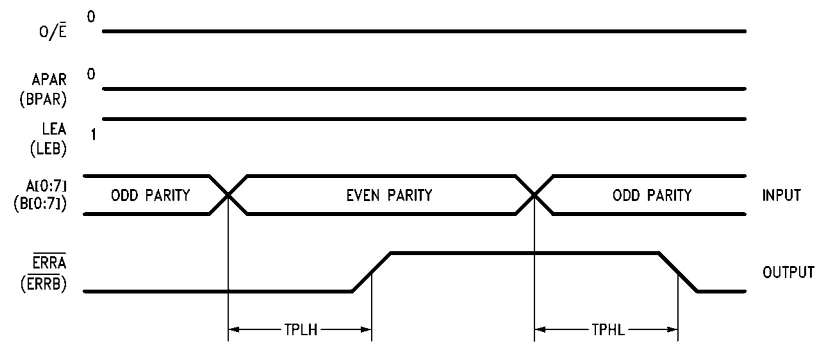
FIGURE 1.



A_n → BPAR

(B_n → APAR)

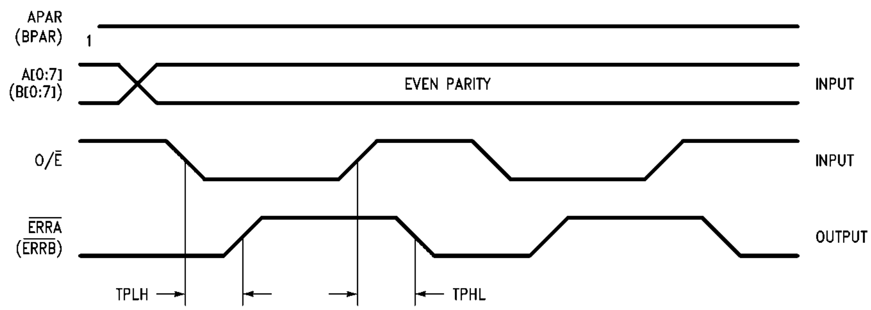
FIGURE 2.



A_n → $\overline{ERRA}$

(B_n → $\overline{ERRB}$)

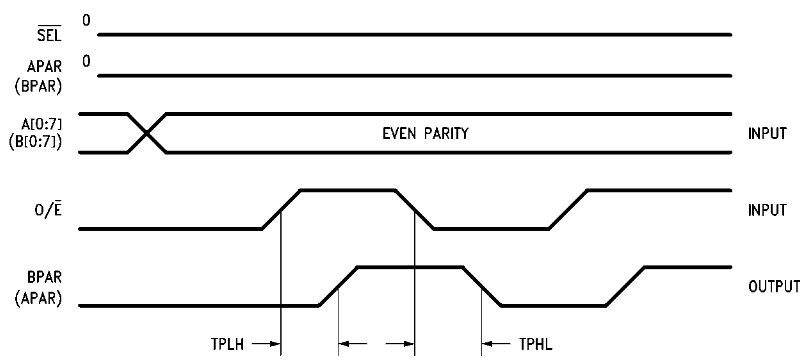
FIGURE 3.



O/$\overline{E}$ → $\overline{ERRA}$

O/$\overline{E}$ → $\overline{ERRB}$

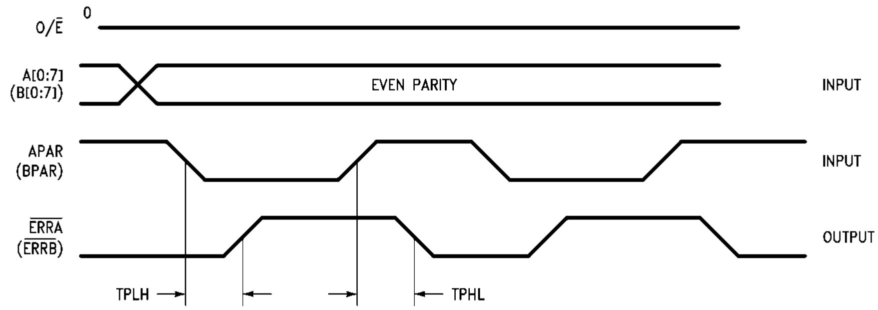
FIGURE 4.



O/$\overline{E}$ → BPAR

(O/$\overline{E}$ → APAR)

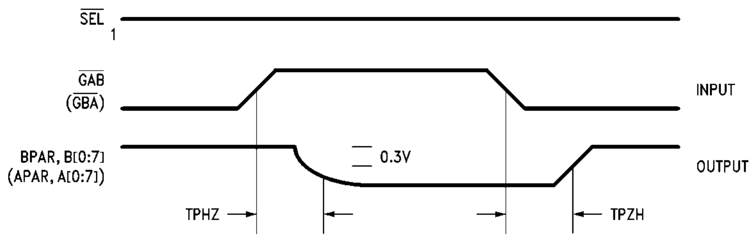
FIGURE 5.



APAR → $\overline{ERRA}$

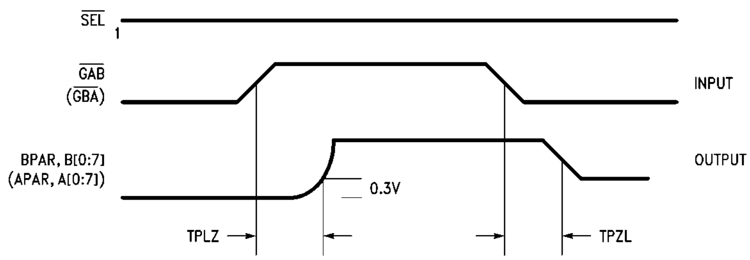
(BPAR → $\overline{ERRB}$)

FIGURE 6.



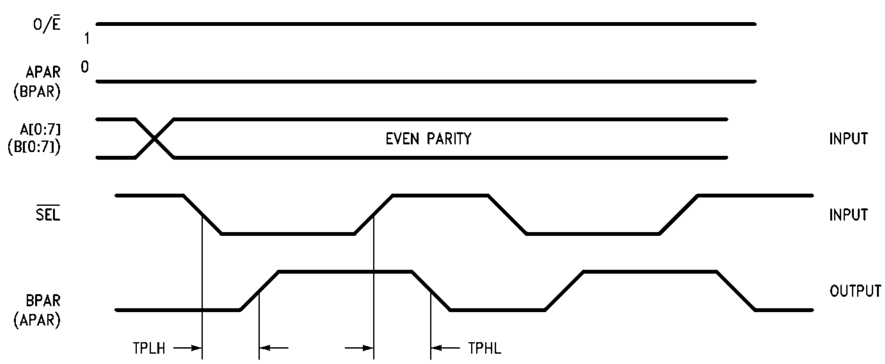
ZH, HZ

FIGURE 7.



ZL, LZ

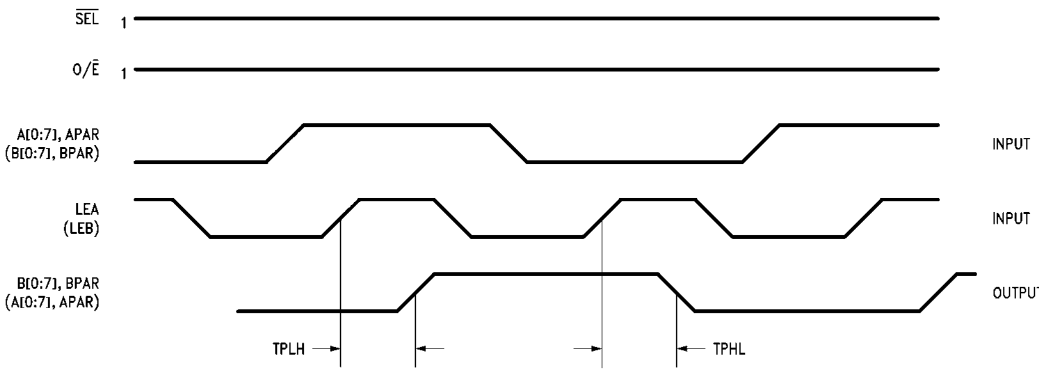
FIGURE 8.



$\overline{SEL}$ → BPAR

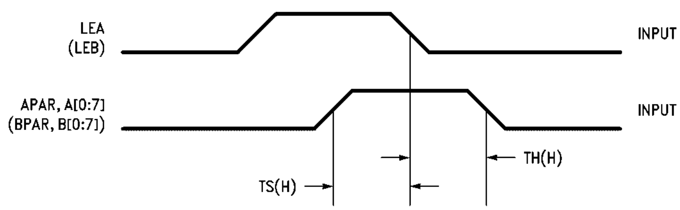
($\overline{SEL}$ → APAR)

FIGURE 9.



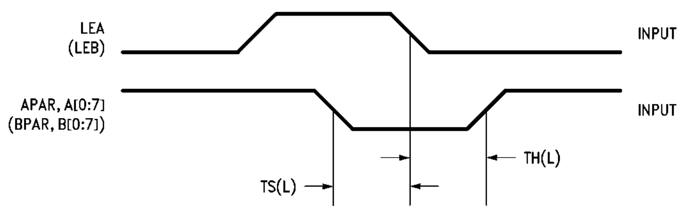
LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

FIGURE 10.



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

FIGURE 11.



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

FIGURE 12.

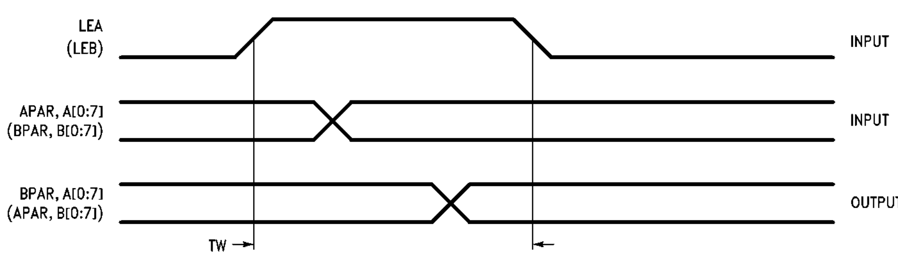


FIGURE 13.

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$	Units	Conditions
				Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$
		5.5	1.5	2.0	2.0		or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$
		5.5	1.5	0.8	0.8		or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50$ µA
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 3)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50$ µA
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 3)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.5	±5.0	µA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 4)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	$V_{IN} = V_{CC}$ or GND

Note 3: Maximum of 9 outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to B_n, A_n	5.0	2.5	7.5	11.5	2.5	12.0	ns	Figure 1
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to BPAR, APAR	5.0	1.5	6.0	8.5	1.5	9.0	ns	Figure 1
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to BPAR, APAR	5.0	2.5	8.5	12.0	2.5	12.5	ns	Figure 2
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.0	8.0	11.5	2.0	12.0	ns	Figure 3
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.0	8.0	11.5	2.0	12.0	ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to APAR, BPAR	5.0	2.5	8.0	11.5	2.5	12.0	ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	5.0	1.5	7.5	10.5	1.5	11.5	ns	Figure 6
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to APAR, BPAR	5.0	1.5	6.5	9.0	1.5	9.5	ns	Figure 9
t_{PLH} t_{PHL}	Propagation Delay LEB to A_n, B_n	5.0	2.5	7.0	10.5	2.5	11.0	ns	Figure 10 Figure 11
t_{PLH} t_{PHL}	Propagation Delay LEA to APAR, BPAR	5.0	2.0	8.0	11.5	2.0	12.0	ns	Figure 10 Figure 11
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.5	8.0	11.5	2.5	12.0	ns	Figure 12
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$ or $\overline{GAB}$ to A_n, B_n	5.0	2.5	7.0	10.5	2.5	11.0	ns	Figure 7 Figure 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$ or $\overline{GAB}$ to BPAR or APAR	5.0	1.5	6.0	9.0	1.5	9.5	ns	Figure 7 Figure 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{GBA}$ or $\overline{GAB}$ to A_n, B_n	5.0	1.5	6.5	9.5	1.5	9.5	ns	Figure 7 Figure 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{GBA}$ or $\overline{GAB}$ to BPAR, APAR	5.0	1.5	6.5	9.5	1.5	9.5	ns	Figure 7 Figure 8

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

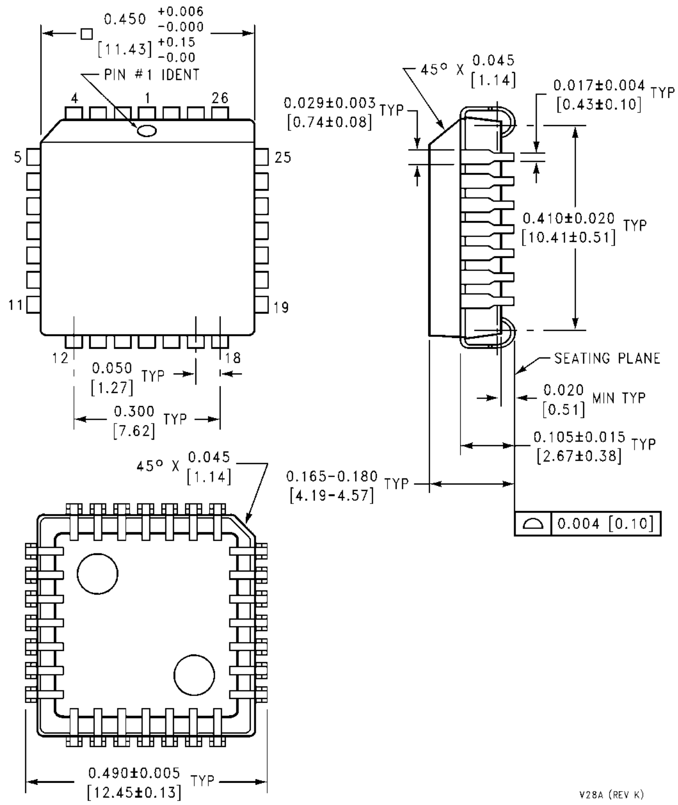
Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = +25°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	5.0	3.0	3.0	ns	Figure 11 Figure 12
t_H	Hold Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	5.0	1.5	1.5	ns	Figure 11 Figure 12
t_W	Pulse Width for LEB, LEA	5.0	4.0	4.0	ns	Figure 13

Note 6: Voltage Range 5.0 = 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	210	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450" Square
Package Number V28A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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